MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

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MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

Summary

This contract seeks to develop a family of thin-film stimulating arrays for use in neural prostheses. STIM-2B/-3B are two- and three-dimensional arrays of stimulating sites on 400µm centers. The probes have four channels and 64-sites. Any selected site can be used for either recording or stimulation. Current generation is off-chip. This probe design has now been completed, with 3D arrays of the STIM-3B probes formed in arrays as large as 1024 sites (256 shanks and 64 parallel data channels, accessible over just eleven external leads). The high-end probes STIM-2/-3 are similar except they use on-chip current generation via 8-bit digital to analog converters. They are accessible over seven external leads.

During the past quarter, research focused on an examination of techniques for reducing the circuit area on the active stimulating arrays and on the realization of an active wireless interface for the probes. With a circuit area of 2.5mm x 5.8mm in the UM 3µm BiCMOS process, the vertical clearance above the cortex is excessive for chronic implants using our usual approach. Folding the probes over so that the circuitry is parallel to the cortical surface, stacking the different layers vertically, is one option being investigated. In parallel, we are exploring other options, including moving some of the circuitry to the platform. All of these options entail a substantial increase in the number of lead transfers required between the probe and the platform, however. Scaling the circuit technology down would help the situation and could give a circuit height of less than 1mm using a 1µm industrial process. We are currently designing a foundry-compatible version of the STIM-2 probe process based on the AMI 1.5µm process; the chip will be fabricated during the coming term. In the meantime, we are exploring a variety of designs for the current DACs used to drive the stimulating sites. The present DAC is large and employs parallel-connected unit transistors to scale the segment currents over a biphasic 8b range (0 to ±127µA). The use of series- as well as parallel-connected transistors can save considerable area, and the use of ratioed transistor sizes with one transistor per segment saves even more. Trading accuracy for area may be a good choice for these circuits.

The development of a wireless interface for the active stimulating probes is continuing. The high leakage currents sometimes seen from the UM BiCMOS process have been studied in detail and found to be due to the lack of a buried layer in this process, resulting in a very high parasitic collector resistance in the bipolar devices. Altering the npn transistor geometry and deliberately adding base resistance to the structure have been shown to greatly reduce the problem. Diode-connected MOS transistors can also be used in place of the bipolar devices in the rectifier and can yield very good performance. During the coming term, we will test the complete Interestim-1 and Interestim-2 microsystems. We will also develop a transmitter and PC-based command generator to implement a full wireless stimulation system and test it in-vitro.

MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

1. Introduction

The goal of this contract is the development of active multi-channel arrays of stimulating electrodes suitable for studies of neural information processing at the cellular level and for a variety of closed-loop neural prostheses. The probes should be able to enter neural tissue with minimal disturbance to the neural networks there and deliver highly-controlled (spatially and temporally) charge waveforms to the tissue on a chronic basis. The probes consist of several thin-film conductors supported on a micromachined silicon substrate and insulated from it and from the surrounding electrolyte by silicon dioxide and silicon nitride dielectric films. The stimulating sites are activated iridium, defined photolithographically using a lift-off process. Passive probes having a variety of site sizes and shank configurations have been fabricated successfully in past contracts and have been distributed to a number of research organizations nationally for evaluation in many different research preparations. For chronic use, the biggest problem associated with these passive stimulating probes concerns their leads, which must interface the probe to the outside world. Even using silicon-substrate ribbon cables, the number of allowable interconnects is necessarily limited, and yet a great many stimulating sites are ultimately desirable in order to achieve high spatial localization of the stimulus currents.

The integration of signal processing electronics on the rear of the probe substrate (creating an "active" probe) allows the use of serial digital input data that can be de-multiplexed on the probe to provide access to a large number of stimulating sites from a very few leads. Our goal in this area is to develop a family of active probes capable of chronic implantation in tissue. For such probes, the digital input data must be translated on the probe into per-channel current amplitudes that are then applied to tissue through the sites. Such probes generally require five external leads, virtually independent of the number of sites used. As discussed in previous reports, we have designed a series of active probes containing CMOS signal processing electronics. Two of these probes have been completed and are designated as STIM-1A and STIM-1B. A third probe, STIM-2, is now beginning a final iteration and is a second-generation version of our original high-end first-generation design, STIM-1. All three probes provide 8-bit resolution in digitally setting the per-channel current amplitudes. STIM-1A and -1B offer a biphasic range using ±5V supplies from 0μA to ±254μA with a resolution of 2μA, while STIM-2 has a range from 0 to ±127μA with a resolution of 1μA. STIM-2 offers the ability to select 8 of 64 electrode sites and to drive these sites independently and in parallel, while STIM-1A allows only 2 of 16 sites to be active at a time (bipolar operation). STIM-IB is a monopolar probe, which allows the user to guide an externally-provided current to any one of 16 sites as selected by the digital input address. The high-end STIM-2 contains provisions for numerous safety checks and for features such as remote impedance testing in addition to its normal operating modes. It also offers the option of being able to record from any one of the selected sites in addition to stimulation. It will be the backbone of a multi-probe three-dimensional (3D) 1024-site array (STIM-3) now in development. A

new probe, STIM-2B, has recently been added to this set. It offers 64-site capability with off-chip generation of the stimulus currents for four separate channels. These channels are organized in four groups so that each current can be directed to any of the 16 sites in its group. Each selected channel can be programmed for either stimulation or recording. On-chip recording amplifiers offer a gain of 50; alternatively, the neural activity can be recorded using off-chip amplifiers interfaced through the normal stimulating channels. This probe is available in both 2D and 3D versions (as STIM-2B/3B) and is now being used in-vivo.

During the past quarter, we have focused work on examining circuit size-reduction for the STIM-2 and STIM-3 probes as well as realization of the first wireless interface for them. The results of these efforts are described more fully in the sections below.

2. STIM-2/3: A Multiplexed Stimulating Probe with On-Chip Current Generation

As noted in previous quarterly reports, we have redesigned our high-end 64-site 8-channel stimulating probes in two- and three-dimensional versions (STIM-2/-3). During the last quarter, we completed the release and testing of the first set of these probes. The modified probe has seven external leads (VDD, GND, VSS, CLK, STB, Data In, and Data Out. It features a new digital-to-analog converter (DAC) with improved performance as well as extensive self-test capabilities to allow the probe to be tested automatically prior to microassembly in 3D arrays (STIM-3). The probe is configured with eight shanks spaced laterally 400µm apart, with the eight sites on each shank spaced at 200µm intervals in depth. In Fig. 1, three pictures of the new probes are shown. The dielectric compensation technique reported previously prevented the backend circuitry from being undercut during the release etch. Figure 2 shows pictures of the back (circuit) areas of the 2D and 3D probes. Since these probe are released along with much smaller recording probes (integrated on the same mask), this corner compensation plays a very important role in achieving high yield across the entire wafer. There are some dielectric lines left along the folding cables of the 3-D probe as can be seen from the bottom picture in Fig. 2; they can be easily removed.

The backend circuit area measures 5.8mm by 2.5mm, which is probably too large for use in guinea pig. We will explore various fold-down configurations during the next quarter, since these are one solution to the die-area problem. However, in any case it is important to shrink the size of the circuit area without sacrificing performance. Accordingly, we are also exploring process, circuit, and system partitioning changes. A MOSIS chip containing the backend circuitry is under development, both to verify full circuit operation of this chip and to explore a hybrid circuit implementation. This chip will also be useful for use with 2D passive probes. The AMI 1.5µm process will be used for this hybrid chip and will support the ±5V supply voltages required. Compared with the UM 3µm single-metal process, the MOSIS circuitry is expected to be much smaller than the present probe back end.

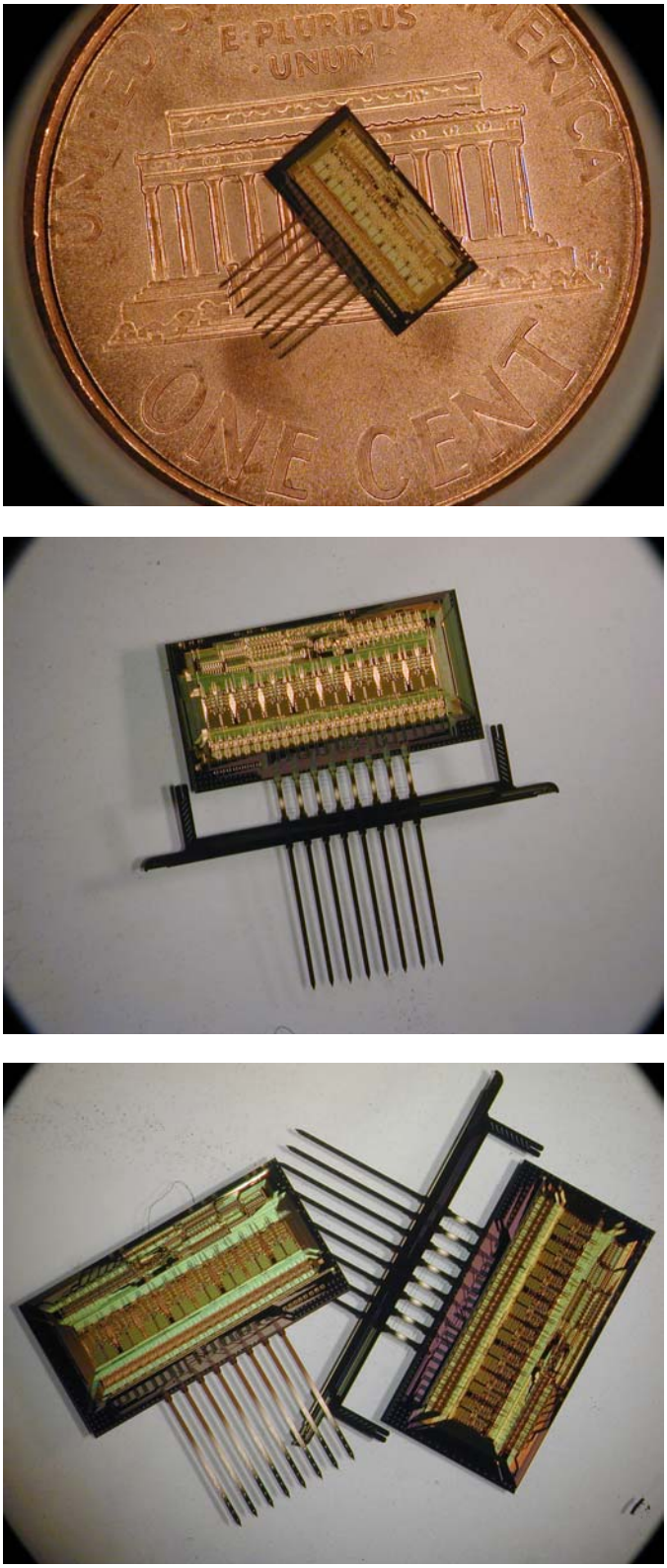


Fig. 1: From top to bottom, the STIM-2 probe is shown on a US penny, the STIM-3 probe, and both probes together.

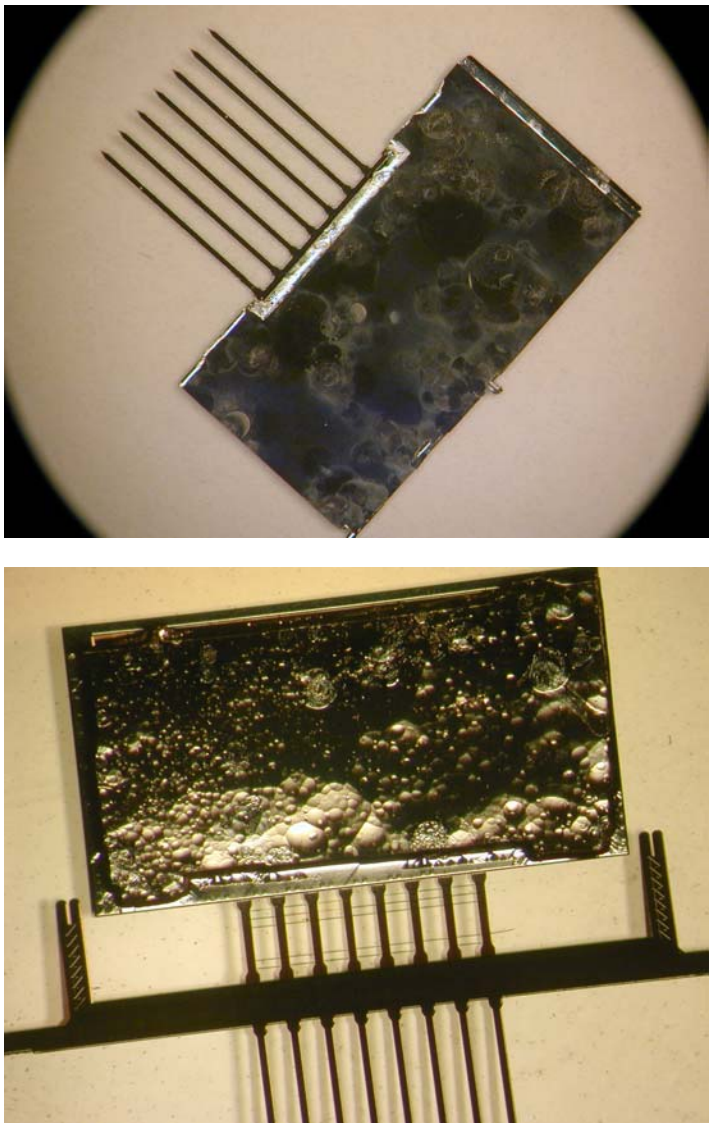


Fig. 2: Pictures of the backs of the 2D (above) and 3D (bottom) probes, STIM-2 and STIM-3.

Another way of attacking the circuit area problem is to move some of the circuitry to the platform, leaving some on the probe instead of trying to use totally passive probes. This can cut down the number of lead transfers required on the platform. Table 1 lists some of the circuit partitioning trade-offs. Moving the 8b digital-to-analog converters (DACs) from the probe to the platform saves both area and lead count. On the other hand, the number of the pads and routing lines on the platform will increase substantially for large probe arrays. Complexity will also be added to the microassembly process since a great many more bonds will be needed on the platform. None of these options appears very attractive due to the large associated per-probe lead counts. We are continuing to explore this problem.

The current DAC can also be designed to reduce its layout area. For better linearity, multiple transistors of the same dimensions are currently used in parallel to obtain binary-coded currents. So for the second branch, 2 unit transistors are placed in parallel; for the third branch, there are 4 unit transistors and so on. For the seventh branch, 64 unit transistors are used in parallel. The total DAC requires 127 transistors. If the unit transistors are instead used in both parallel and series then for the first branch, 8 unit transistors are in series; for the second, 4 in series; for the third, 2 in series; for the fourth, just one unit transistor; for the fifth, 2 unit transistors in parallel; for the sixth, 4 in parallel and for the seventh, 8 in parallel. Here we need only 29 transistors for the DAC. Thus, the layout area can be greatly reduced at some cost in performance. Figure 3 shows a comparison of the current sourcing and sinking capabilities of these two designs. Since the series/parallel DAC has more transistors cascaded, more voltage is required to keep the sources saturated, as shown in Fig. 4.

Circuitry on the probe	**Number of lead transfers, probe to platform**	
None (totally passive)	64	
Front-end Selector only	36	8 input current lines
		8 channel-select lines
		8 site select lines
		1 output data lines
		3 power lines
		8 test-site-select lines
Front-ened Selector + Decoders	25	13 decoding lines for
		8 input current lines
		1 output data line
		3 power lines
Selector + Decoder + Shift-register	14	8 input current lines
		1 clock line
		2 data lines (in, out)
		3 power lines
Full Circuit Implementation	7	current design

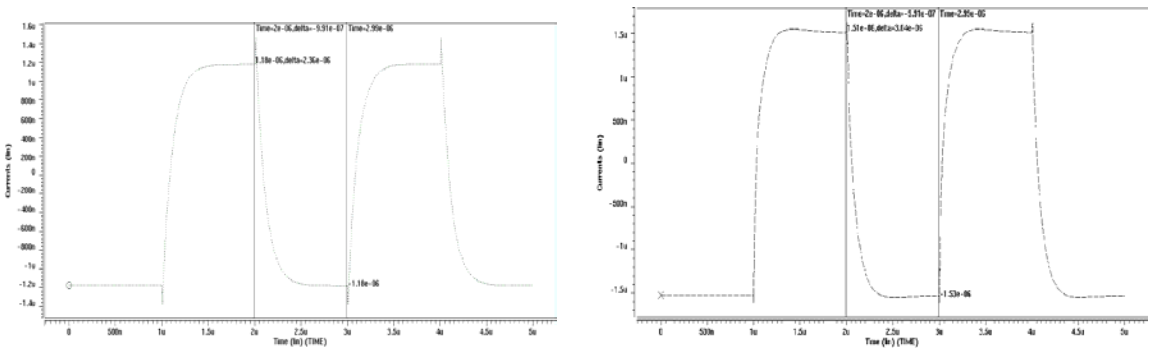


Fig. 3: Simulation of the current sourcing and sinking performance of the two DAC designs (left: for all-parallel DAC; right: series/parallel DAC)

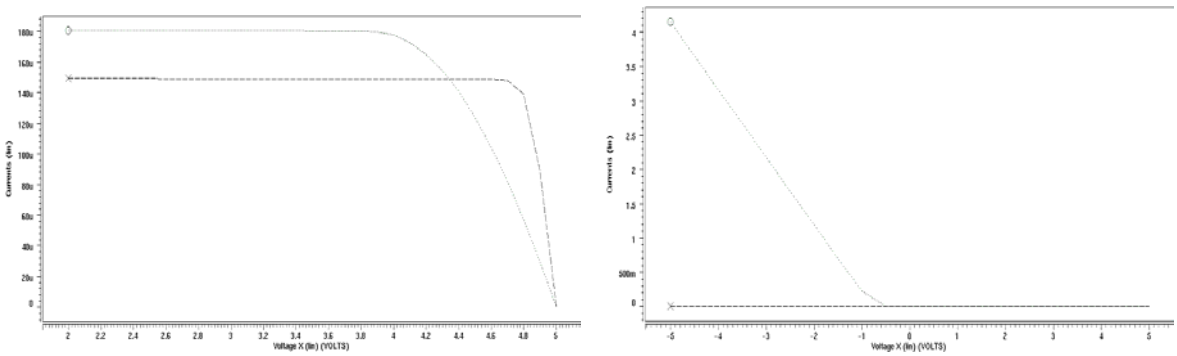


Fig. 4: DAC output current as a function of output voltage (left: sourcing current; right: sinking current; dashed line: all-parallel DAC; dotted line: series/parallel DAC)

In the left figure of Fig. 4, the output is a full-scale sourcing current; the output voltage varies from 2V to 5V. The previous design, corresponding to the dashed line, shows a higher output resistance. In the right figure, where the output is a full-scale sinking current and the output voltage varies from –5 to 5V, the series/parallel DAC design corresponding to the dotted line gives poor performance. But as shown in Fig. 5, the simple current source DAC corresponding to the red solid line (which was used in the original version of STIM-2) gives no better performance. A final design to be considered uses a single transistor per segment with ratioed channel dimensions. This should give the smallest overall layout area; performance must still be evaluated. Although matching will presumably be more of a problem, we suspect that absolute accuracy is not a prime requirement for this application. Accuracy may be a good thing to trade for area here.

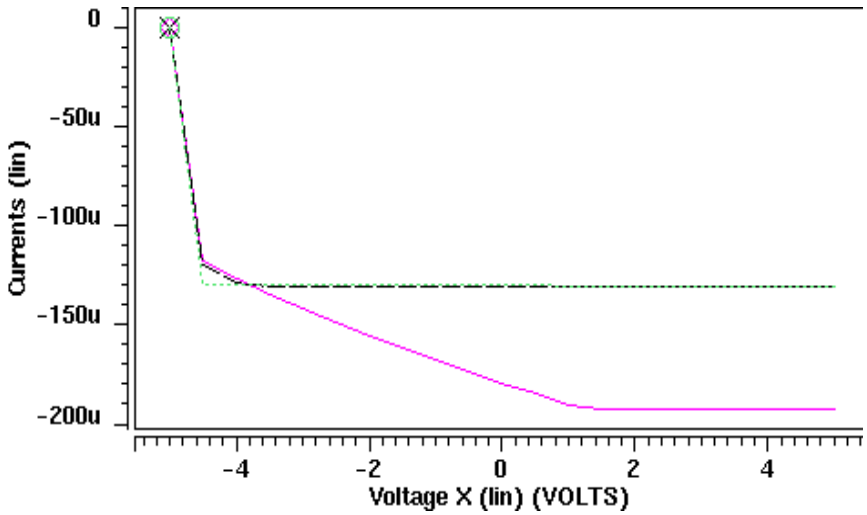


Fig. 5: Output sink current versus output voltage (solid line: simple current source; dotted line: conventional cascode DAC; dashed line: the current design)

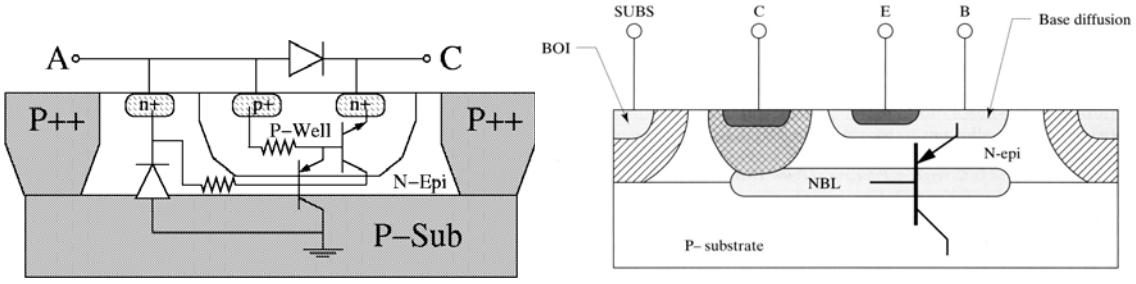
3. A Wireless CNS Stimulating System

The University of Michigan's most recent single-metal dual-poly 3µm BiCMOS process run was finished during the past quarter, and characterization of the individual devices and circuits in these Interestim chips is underway. We are going to use some of the fully-functional chips in a larger system, putting together different components to form a wireless stimulating microsystem including transmitter circuitry, receiver/ transmitter coils, and a PC-based command generation station. This report will describe the characterization that has taken place to date.

Leakage Current in the UM BiCMOS Bipolar Junction Transistors

The UM BiCMOS circuits have always suffered from excessive leakage current in the associated BJT's, especially when they must handle large amounts of current, as in the BJT rectifier block. However, there have been no previous studies specifically targeted at overcoming this problem. Having a good understanding of this problem is important in designing a low power wireless microsystem. Therefore, we have examined this issue in more detail during the past term.

The source of leakage current in the UM BiCMOS process is evident comparing the cross-sections of a vertical NPN transistor in this process with one in a standard BiCMOS process, as shown in Fig. 6. Two major differences between the UM and standard BiCMOS transistors are the lack of an n^+ buried layer to minimize the lateral collector resistance in the UM process and lack of a deep N+ plug to minimize the



(a) (b)

Fig. 6: Comparison of the cross-sections of a UM BiCMOS vertical NPN transistor and a similar device in a standard BiCMOS process.

vertical collector resistance. These two deficiencies, which are imposed by the process, deteriorate the performance of the NPN devices by increasing the collector parasitic resistance. Fig. 6a shows cross section of a diode-connected UM NPN transistor with its associated parasitic components. Here, the N-epi and P-well are shorted to prevent the parasitic PNP transistor from turning on. However, when the diode is forward biased, current passes through P-well and turns the original NPN on. This in turn passes some of the diode forward current through the N-epi, which has a high resistivity under the P-well region because of the lack of n^+ buried layer in this process. If the voltage drop across the N-epi resistor exceeds V_{BE}(on), the parasitic PNP transistor turns on, resulting in current leakage from P-well to the grounded P-substrate. Changing the UM BiCMOS

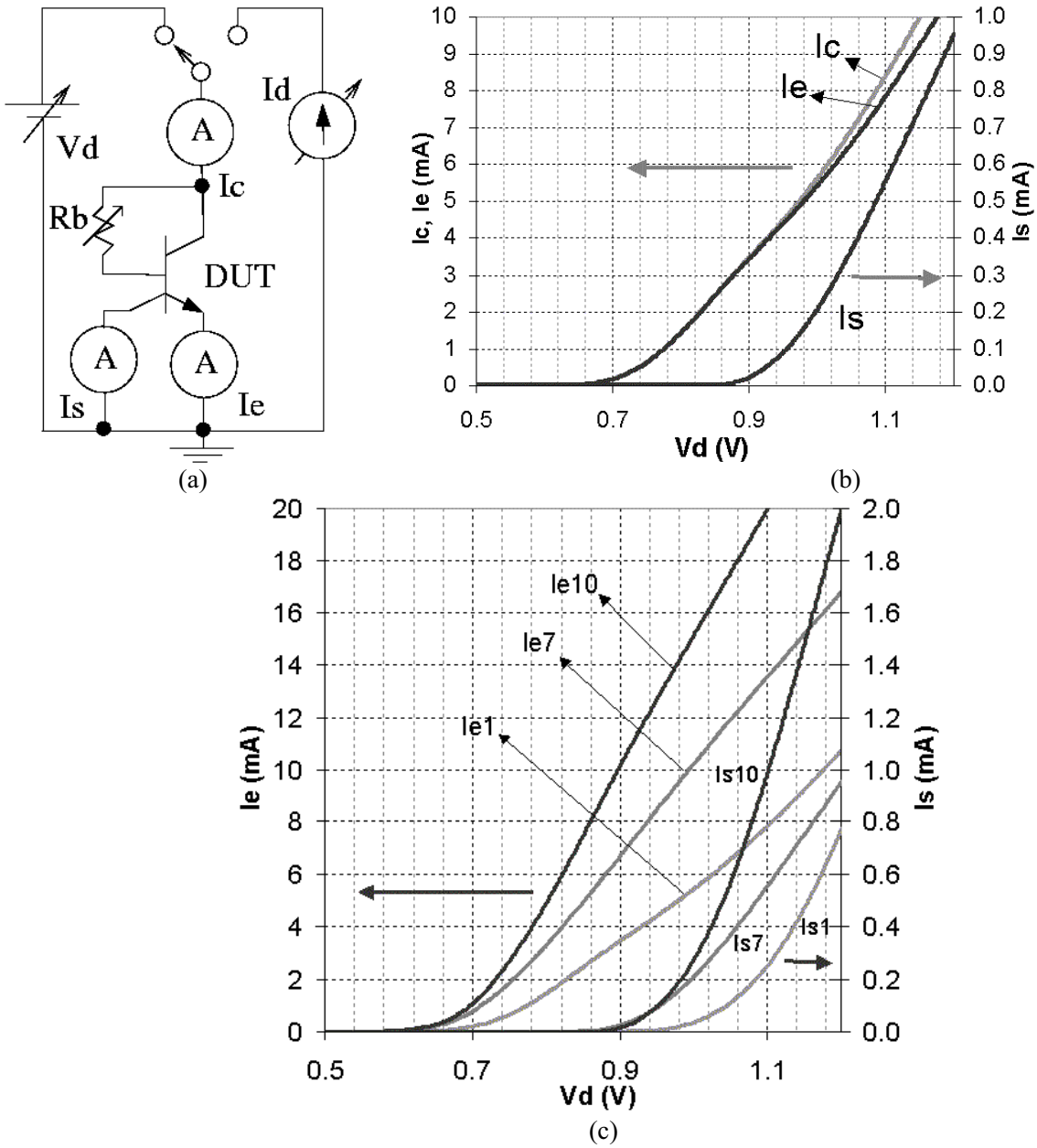


Fig. 7: (a) Substrate leakage current test circuit; (b) Substrate leakage current (I_s) compared to the emitter current (I_e) when the diode voltage is increased; c) The effect of diode-connected NPN emitter size on substrate leakage current (D1: 7x37µm; D7: 7xD1; D10: 10xD1)

process, which has been optimized for fabricating the neural probes over a number of years was not an attractive option; therefore, two other methods were examined in order to decrease the substrate leakage current.

1) *Increasing the diode-connected NPN geometry:* This method puts several of N-epi distributed resistors in parallel, resulting in a reduction of their overall value. The minimum-size NPN transistor emitter size, so called NPN1, was chosen to be 7µm x 37µm. The diode-connected NPN1, so called D1, was forward biased as shown in Fig. 7a and V_d was changed from 0.5V to 1.2V while measuring I_c, I_e, and the substrate leakage current I_s. The resulting curves in Fig. 7b show that I_s becomes significant when I_d>3mA. However, this is not enough for many applications, including our wireless neural stimulator. To test the effect of diode geometry on the leakage current, two other diode-connected NPN transistors, D7 and D10, with emitter areas 7 and 10 times larger than D1, were compared in a similar way. The results shown in Fig. 7c agree with our speculation, showing that D10 can pass up to 10mA without significant substrate leakage. The

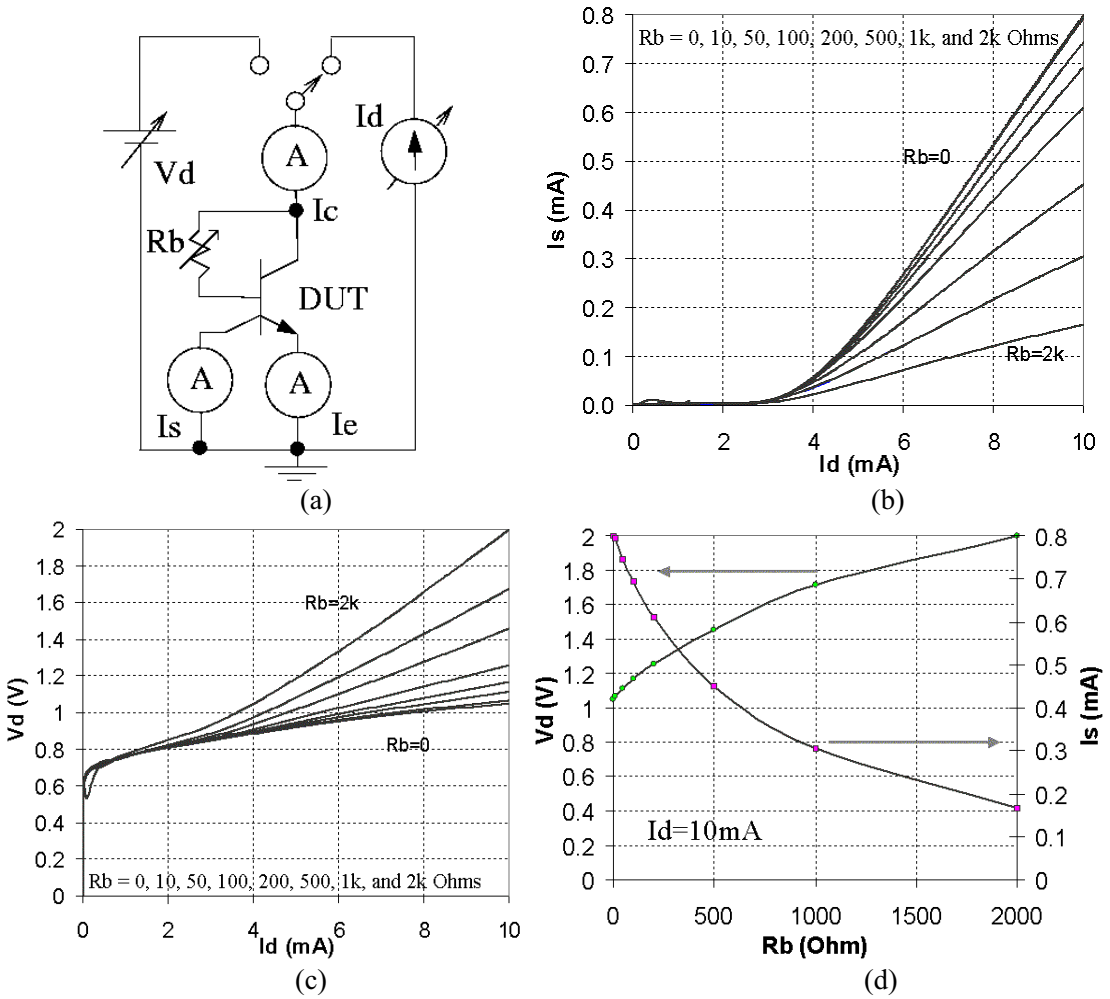


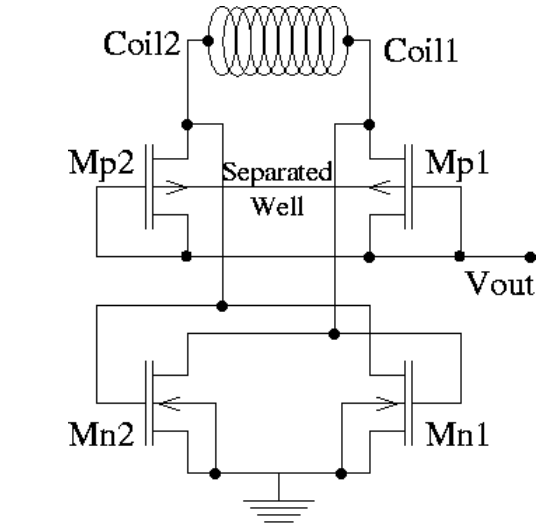
Fig. 8: The effect of base resistance (R_b) on diode-connected NPN substrate leakage current. a) Substrate leakage current test circuit. b) Substrate leakage current when R_b is changed from 0 to 2kΩ. c) Diode-connected NPN voltage drop. d) Comparison between the desirable substrate leakage current reduction and undesirable diode voltage drop increase by increasing R_b when diode current is fixed at 10mA.

disadvantages of using larger diodes are more chip area consumption and increasing diode parasitic capacitance, which can result in poor high frequency performance and significant voltage drop at the 4MHz carrier frequency.

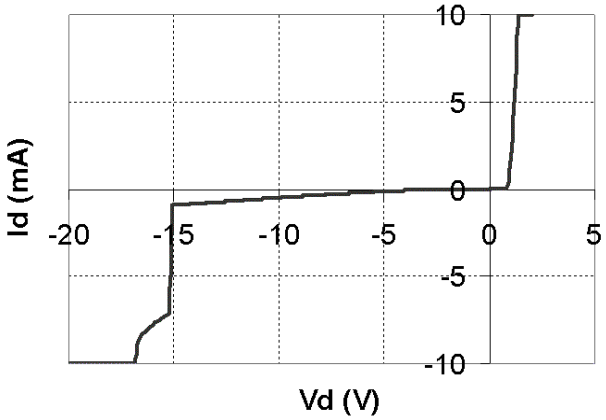
2) *Adding a base resistor:* Fig. 6a shows that the vertical NPN base is the emitter node for the parasitic vertical PNP, which is responsible for the substrate leakage. Therefore, it suggests that adding more base resistance in the leakage current path while keeping the collector resistance constant in the main forward current path can reduce substrate leakage. This was tested on D1 by switching to a current source, I_d and changing R_b in Fig. 8a from 0 to 2kΩ. The results are shown in Fig. 8. Fig. 8b shows that the leakage current has been decreased significantly especially at high currents. For example at I_d=10mA, I_s has been reduced to less than a quarter of its initial value from 0.8mA to 0.16mA as shown in Fig. 8d. However, the disadvantage of this method is increasing the diode forward voltage drop, which is shown in Fig. 8c. Fig. 8d shows that the diode forward voltage drop increases from 1.05V to 2.0V when R_b changes from 0 to 2kΩ and I_d=10mA. Therefore, even though adding a base resistor saves power in reducing the substrate leakage current, it dissipates more power in rectifier diodes and increases the required minimum operational coil voltage of the wireless implant.

CMOS bridge rectifiers:

To eliminate the substrate leakage current, described in the previous section, diode-connected MOS transistors can be used instead of BJT's to realize a CMOS full-wave bridge rectifier as shown in Fig. 9a. Another advantage of these rectifiers is their compatibility



(a)



(b)

Fig. 9: (a) Simplified schematic diagram of a CMOS full-wave rectifier. (b) I_d-V_d curve for a sample diode-connected PMOS implemented in the AMI 1.5µm standard CMOS process with W/L=4800/1.6

with a standard CMOS process, which is more popular and cost effective than BiCMOS. The structure of these rectifiers was shown in the previous report and will be discussed in

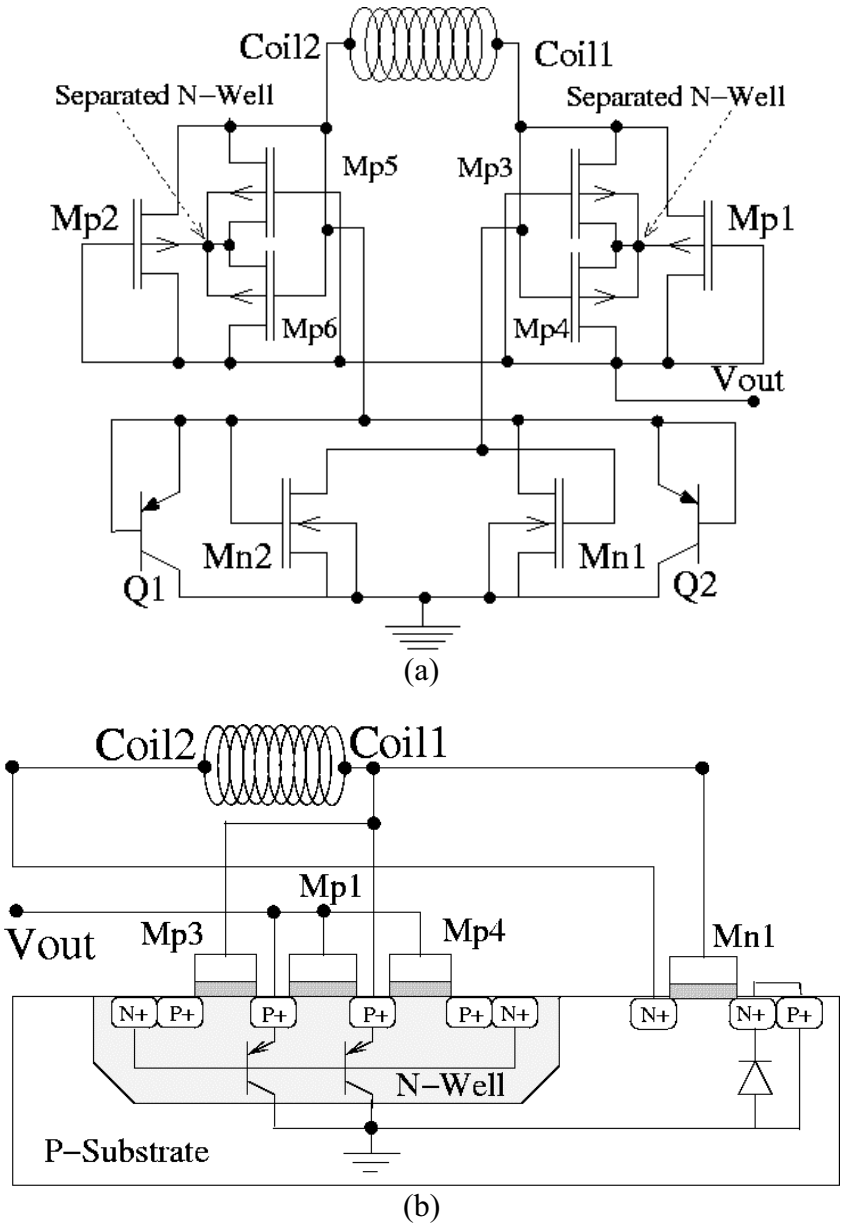


Fig. 10: (a) Schematic diagram of the CMOS full-wave rectifier. (b) Cross section of half of the CMOS full-wave rectifier showing the diode-connected PMOS complex and parasitic PNP transistors.

more detail here. M_{P1} and M_{P2} conduct in the forward direction when coil voltage is higher than V_{out}, delivering power from the coil to the load. Current passes through the load to grounded P-substrate and returns back to the coil from M_{N1} and M_{N2}, which work as switches controlled by the coil voltage. The instantaneous voltage drop on a diode-connected MOS when current I_D is passing trough it can be found from:

$$\left|V_{GS}\right| = \left|V_{DS}\right| = \left|V_{Th}\right| + \sqrt{\frac{2I_D}{\mu C_{ox}\left(W/L\right)}} \qquad (1)$$

The MOS threshold voltage, V_{TH}, is basically a process dependent parameter and can be minimized in the circuit design by eliminating the body effect. To minimize the second term, the W/L ratio should be increased as much as area consumption and parasitic capacitance allow. Reducing the rectifier voltage drop decreases power dissipation in the rectifier block and increases the average rectified DC voltage available at the regulator block input, lowering the implant required minimum operational input voltage. Fig. 9b shows I_d-V_d curve for a sample diode-connected PMOS implemented in AMI 1.5µm standard CMOS process with W/L=4800/1.6. The substrate leakage is not significant except where the reverse diode voltage is close to the diode breakdown.

Since the sources of all rectifier MOS transistors in Fig. 9a are connected to the coil terminals, which have large voltage variations at high frequency, protecting this circuit against latch-up and substrate leakage current is crucial. The separated N-Well in Fig. 9a schematic is one of the points that increase the risk of substrate leakage current by turning on the parasitic vertical PNP when the coil voltage goes above V_{out} if the N-well potential is not properly controlled. In order to dynamically control the separated N-well potential to reduce possibility of latch-up and substrate leakage, two auxiliary PMOS transistors were added to each rectifying PMOS to connect the N-well to V_{out} or the coil terminal either has a higher potential. The resulting rectifier circuit is shown in Fig. 10 with half of its symmetrical cross section demonstrating the diode-connected PMOS complex and parasitic PNP transistors. The source-side auxiliary PMOS (M_{P3}) shares the source and the gate with the diode-connected M_{P1} and turns on whenever M_{P1} is ON, connecting the separated N-well to the coil voltage, which is higher than V_{out}. The drain-side auxiliary PMOS (M_{P4}) shares the drain with M_{P1} and turns on whenever M_{P1} is OFF connecting the separated N-well to the output voltage, which is higher than the coil voltage at this time. Since no current passes through auxiliary MOSFET's when they turn on, their drain-source voltage is close to zero. Therefore, they do not let the parasitic vertical PNP transistors to turn on and leave little chance for leakage current or latch-up. Another advantage of this configuration is eliminating the body effect on the rectifying PMOS transistors that reduces the rectifier voltage drop and power dissipation as mentioned above. On the NMOS transistor side, vertical PNP transistors are used in parallel to M_{N1} and M_{N2} to return the current back to the coil when its potential goes below grounded substrate. A prototype version of this rectifier was implemented in the AMI 1.5µm standard CMOS process and fabricated through MOSIS foundry. This 2.2mm× 2.2mm chip, which is shown in Fig. 11, also contains other prototype circuitry such as some regulator designs and an FSK demodulator, which will be covered later. To decrease the risk of latch-up further, the PMOS complexes and the NMOS pair were widely separated and protected by N^+ and P^+ guard rings, respectively.

Implementation of the CMOS rectifier in the UM BiCMOS process was slightly different because here we have more parasitic components. Therefore both rectifier NMOS and PMOS transistor pairs have to be separated from the rest of the circuits and

equipped with auxiliary MOSFETs to prevent leakage current and latch-up. Fig. 12 shows the new CMOS rectifier schematic, a cross-section of half of its sym-metrical structure demonstrating the NMOS and diode-connected PMOS complexes, and a fabricated prototype rectifier. M_{N3} and M_{N4} dynamically control the separated P-well potential and connect it to the lower of either ground or coil voltages, and M_{P3} and M_{P4} dynamically control the separated N-epi potential and connect it to the higher of either V_{out} or the coil voltages. This is shown in simulated waveforms of Fig. 13a. The two upper traces are V_{out} and coil1 voltages and the lower two traces show how separated N-epi and separated P-well voltages follow max(V_{out},Coil1) and min(GND,Coil1), respectively. Figures 13b and 13c show measured waveforms on the prototype CMOS rectifier while connected to a 1kΩ load. These traces are Coil1, separated N-epi, and V_{out} from top to bottom in Fig. 13b. Fig. 13c shows similar waveforms super-imposed to demonstrate their relative amplitudes, which agree with the simulation results in Fig. 13a.

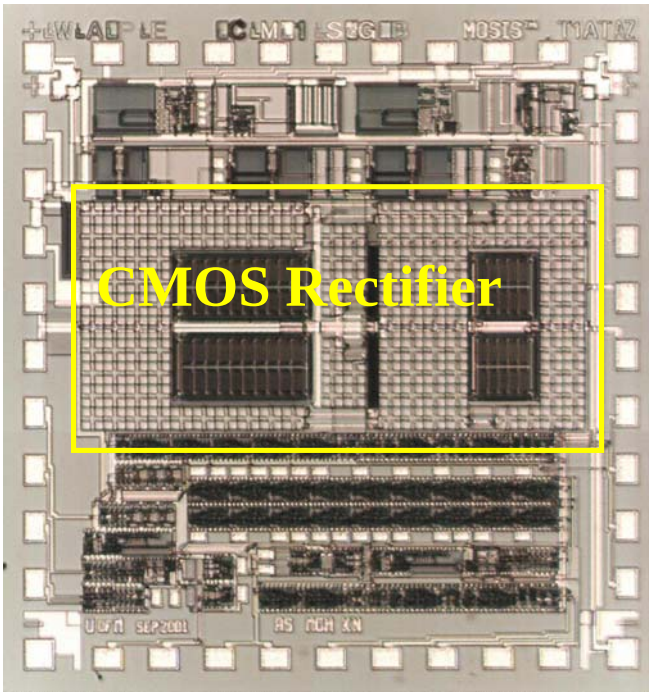
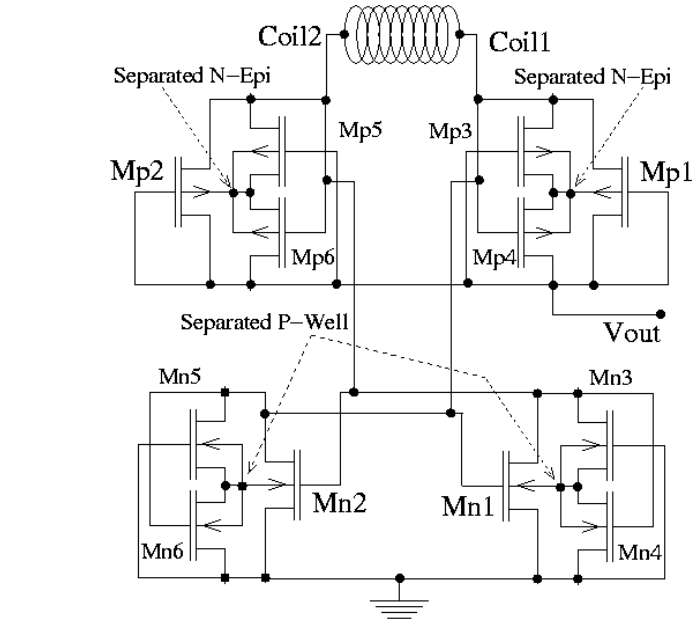


Fig. 11: Photomicrograph of the prototype CMOS full-wave rectifier implemented in AMI 1.5µm standard CMOS process. Die size 2.2x2.2mm.

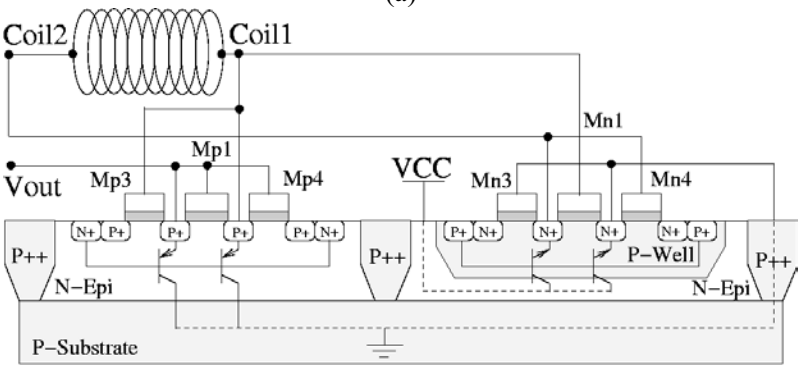
At high frequency, parasitic capacitors should be considered as a limiting factor in setting the size of the rectifier MOSFET's. However, in a complete wireless implant chip most of these capacitors are lumped in parallel with the tank resonant circuit capacitor, connected across the coil input terminals, or the rectifier low pass filter capacitor, connected between the rectifier output and ground terminals. Therefore, their most significant effect is varying these two capacitors, which can be adjusted after fabrication by trimming provisions. The test results show that the CMOS rectifier frequency response is superior to all other BJT counterparts that have been fabricated in the same process.

Power Distribution in the Wireless Stimulating Microsystem

The specific power distribution method in Interestim-1 has been discussed in previous reports and is shown as a reference in Fig. 14. The sinusoidal waveform out of the receiver tank circuit is rectified after passing through a bipolar or CMOS full-bridge rectifier.



(a)



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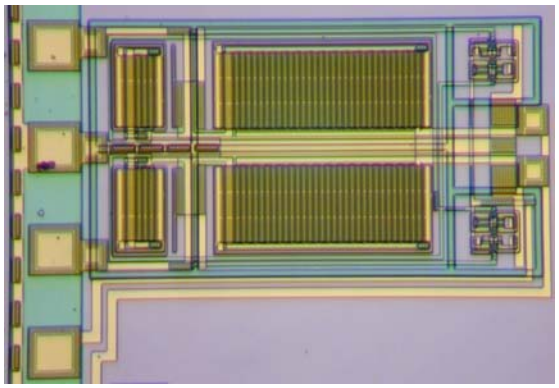
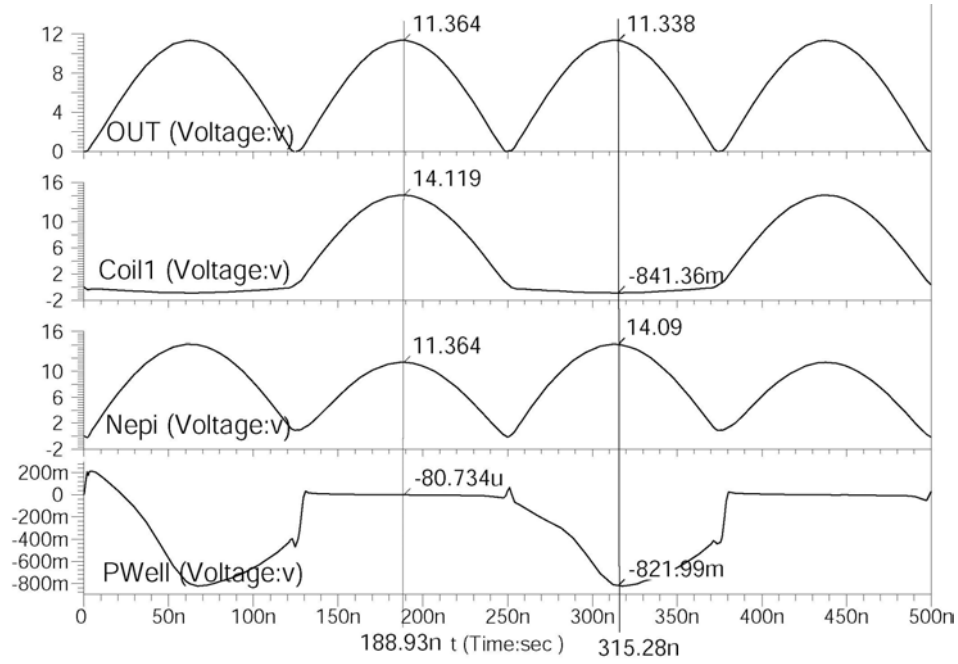


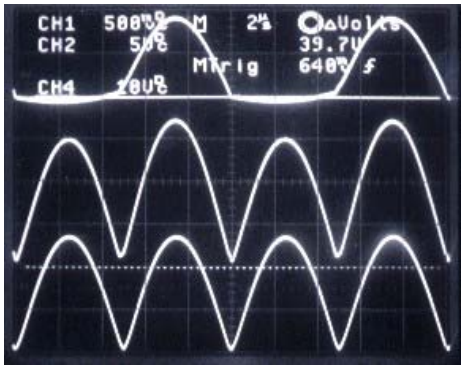
(c)

Fig. 12: (a) Schematic diagram of the CMOS full-wave rectifier implemented in an N-epi BiCMOS process (b) Cross-section of half of the symmetrical structure showing the NMOS and diode-connected PMOS complexes and parasitic BJT's. (c) Prototype rectifier fabricated in the UM 3µm BiCMOS process. Die Size: 0.5mm x 0.73mm

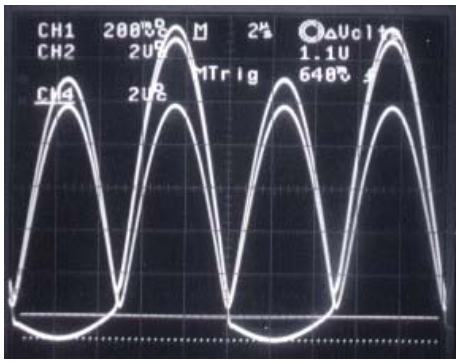
Two types of regulators have been used in our designs, which simplified schematics can be seen in Fig. 14b and 14c. Both regulator designs generate a high current 10V output and a low current 5V reference from a minimum unregulated DC input of 12V. These regulators have been tested functionally and described in the last report.



(a)



(b)



(c)

Fig. 13: Simulation and measured waveforms when the CMOS rectifier is loaded by a 1kΩ resistor. (a) Simulation waveforms from top: Rectified output voltage, one of the coil input voltages, separated N-epi voltage controlled by auxiliary PMOS's, and Separated P-well voltage controlled by auxiliary NMOS's. (b) Measured waveforms from top: Coil input, separated N-epi, and output voltage. (c) Similar measured waveforms superimposed to demonstrate their relative amplitudes.

Class AB Unity-Gain Buffer: By means of a class AB unity-gain buffer, the regulator 10V, 5V, and internal ground become +5V, GND, and –5V power supply rails,

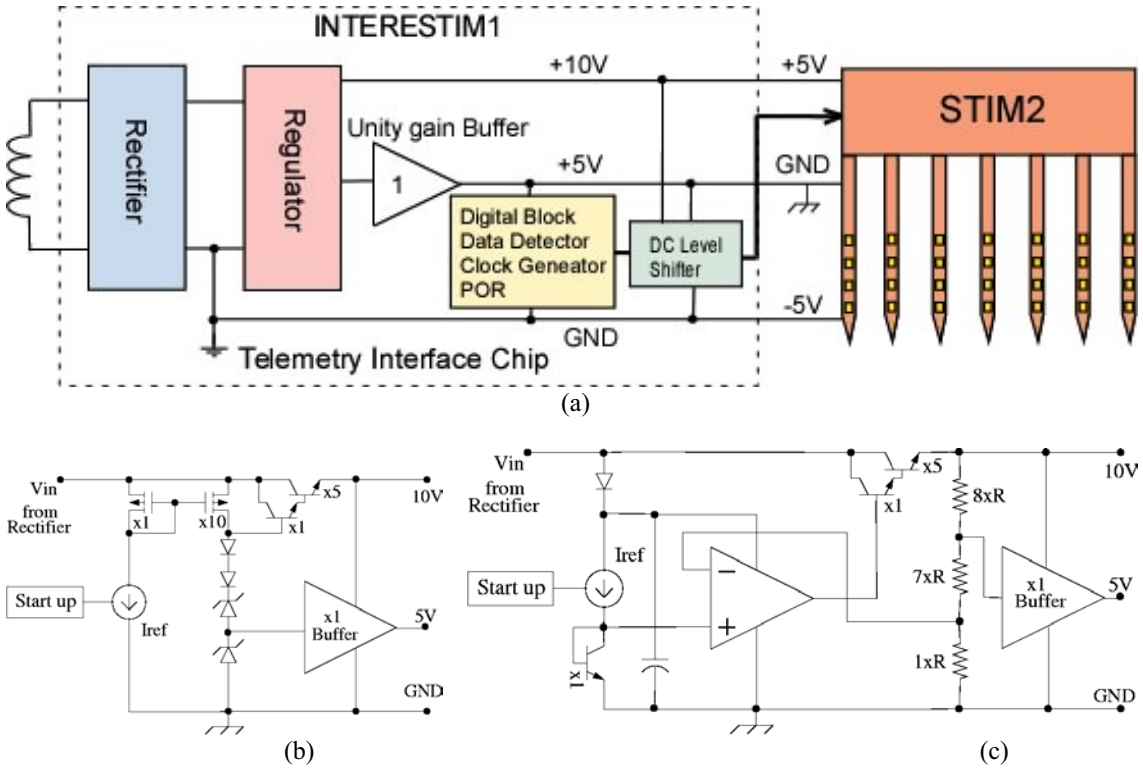


Fig. 14: (a) Power distribution diagram of the wireless stimulating microsystem, consisting of Interestim-1 and STIM-2. (b) Open-loop Zener-referenced voltage regulator block. (c) Closed-loop V_{BE}-referenced regulator block.

respectively, for the stimulator chip (STIM-2). This unity gain buffer, which output should serve as a virtual ground for the next chip, should be able to source and sink as much as 5mA without much variation from its 5V input. A class B output stage seems to be a good choice for the unity gain buffer because of its high current gain and negligible standby power consumption, but since the output should always stay around 5V, the class B amplifier dead-zone generates a lot of ripple on the isolated chip GND rail. Therefore, a class AB output stage was used for the unity-gain buffer. A simplified schematic diagram is shown in Fig. 15. The disadvantage of this circuit, however, is the use of two PNP transistors in it, which show poor performance in our process because of their lateral structure. Therefore, these PNP transistors (Q_2 and Q_4) have been replaced

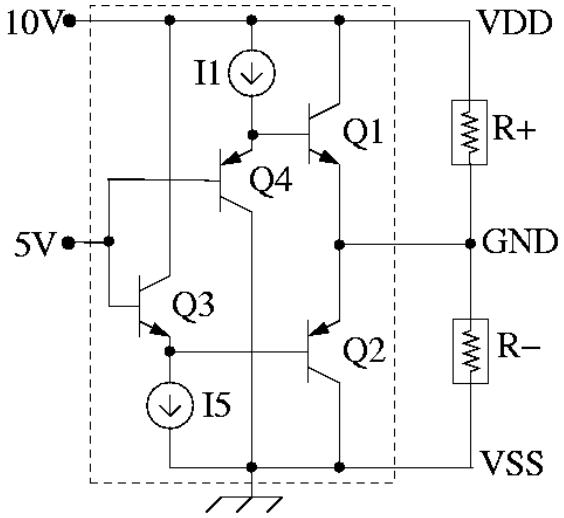


Fig. 15: Simplified schematic diagram of the class AB unity gain buffer.

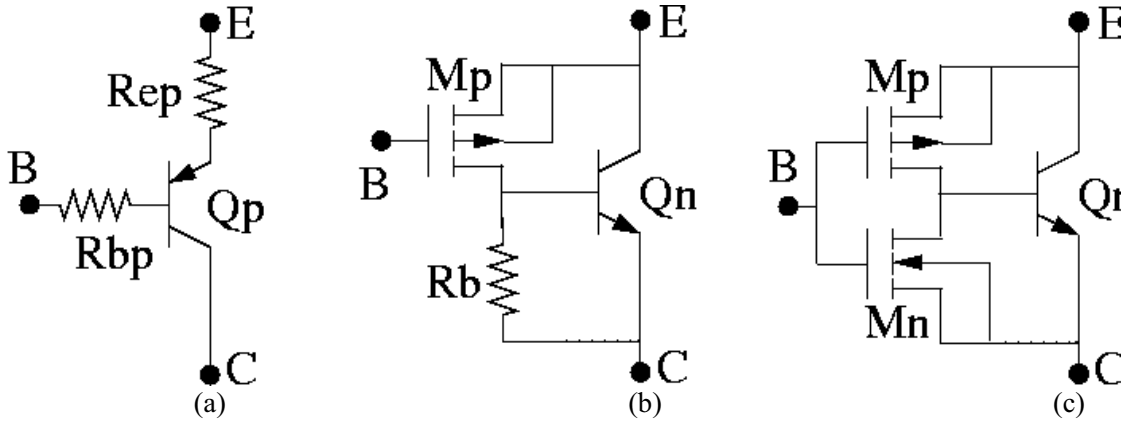


Fig. 16: A PNP transistor and its NPN-PMOS equivalents.

by their PMOS-NPN equivalents that can be seen in Fig. 16. The major difference between a PNP transistor and its PMOS-NPN equivalent is the V_{BE}(on) voltage, which is a weak function of the collector current in the former but is defined from (1) in the latter with I_D replaced by V_{BE}/R_B. To reduce the effect of the second term in (1), we want to increase R_B and the W/L ratio of the PMOS transistor. However, a large R_B, which is found to be in the order of 100kΩ consumes a lot of chip area. Therefore, R_B in Fig. 16b was replaced by an NMOS with small W/L ratio, biased in the triode region. The equivalent R_B can be calculated from:

$$R_B = \left[\mu_n C_{ox}(W_n / L_n)(V_{GS} - V_{ThN} - V_{BE(ON)})\right]^{-1} \qquad (2)$$

Figure 17 compares the simulated (I_E-V_{BE}) curves for the three PNP-equivalent circuits shown in Figure 16 when V_{CE} is kept constant at 2V. These simulations use the transistor models extracted from our BiCMOS process parameters and show how closely circuits 16(b) and 16(c) can follow PNP transistor characteristics of 16(a).

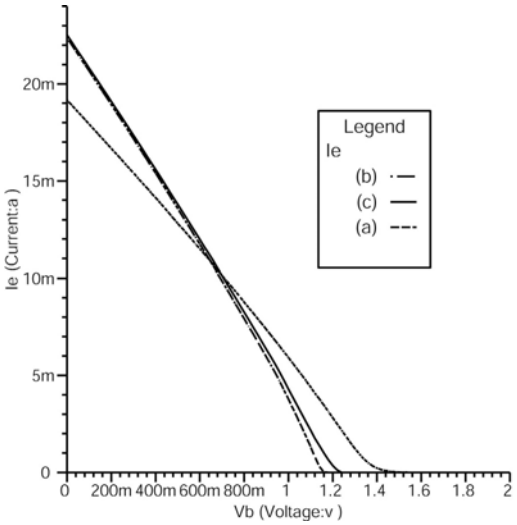


Fig. 17: I_E-V_{BE} curves for the PNP-equivalent circuits shown in Figure 16 when V_{CE} = 2V.

The complete unity-gain buffer schematic is shown in Fig. 18. The internal current consumption, which is designed to be 130μA, is basically due to I_1 and I_5 current sources in Fig. 15, that are implemented by M1 and M5, respectively. It can be shown that the small signal output resistance of the PMOS-NPN compound is

$$R_o = 1/g_{mp}(1 + g_{mn}(R_B \parallel r_\pi)) \approx 1/g_{mp}h_{fe} \qquad (3)$$

where g_{mn} and g_{mp} are M_n and M_p transconductances, respectively, and r_π and h_{fe} are Q_n hybrid π parameters. This output resistance in parallel with the resistance seen from Q_2 emitter is low enough for the unity gain buffer output to source and sink as much as 5mA with less than a 1V variation in its output voltage, which is required for a stable ground node. In order to test this circuit, the unity-gain buffer output has been monitored in both regulator designs, shown in Fig. 14b and 14c, while changing the ratio between the VDD and VSS loading (R+ and R-). Figures 19a and 19b show that the GND baseline variation is less than 0.5V when one of the loads is kept constant at 1kΩ and the other one is changed between 1kΩ and 1MΩ.

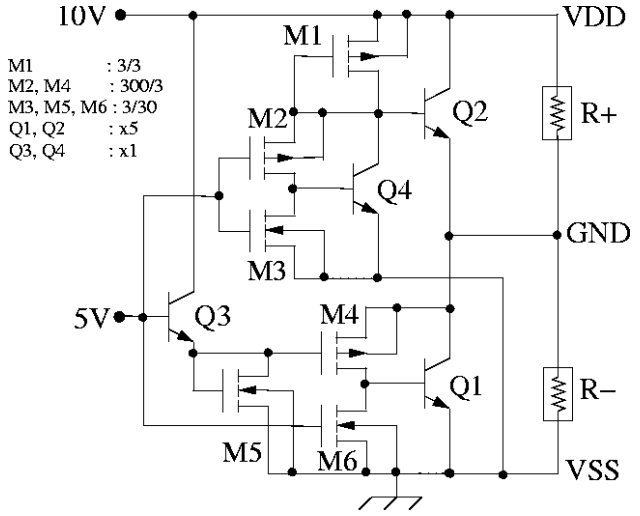


Fig. 18: Simplified schematic diagram of the class AB unity gain buffer.

During the next quarter we will continue testing the individual blocks as well as the complete Interestim-1 and Interestim-2 systems. We are going to work on the transmitter and the PC-based command generator station to implement a true wireless stimulating setup for testing the functionality of our chips in vitro.

4. Conclusions

During the past quarter, research focused on an examination of techniques for reducing the circuit area on the active stimulating arrays and on the realization of an active wireless interface for the probes. With a circuit area of 2.5mm x 5.8mm in the UM 3µm BiCMOS process, the vertical clearance above the cortex is excessive for chronic implants using our usual approach. Folding the probes over so that the circuitry is parallel to the cortical surface and the different layers stack vertically is one option being investigated. In parallel, we are exploring other options, including moving some of the circuitry to the platform. All of these options entail a substantial increase in the number of lead transfers required between the probe and the platform, however. Scaling the circuit technology down would help the situation and could give a circuit height of less than 1mm using a 1µm industrial process. We are currently designing a foundry-compatible version of the STIM-2 probe process based on the AMI 1.5µm process, and the chip will be fabricated during the coming term. In the meantime, we are exploring a variety of designs for the current DACs used to drive the stimulating sites. The present

DAC is large and employs parallel-connected unit transistors to scale the segment currents over a biphasic 8b range (0 to ±127μA). The use of series- as well as parallel-connected transistors can save considerable area and the use of ratioed transistor sizes with one transistor per segment saves even more. The trading of accuracy for area may be a good choice for these circuits.

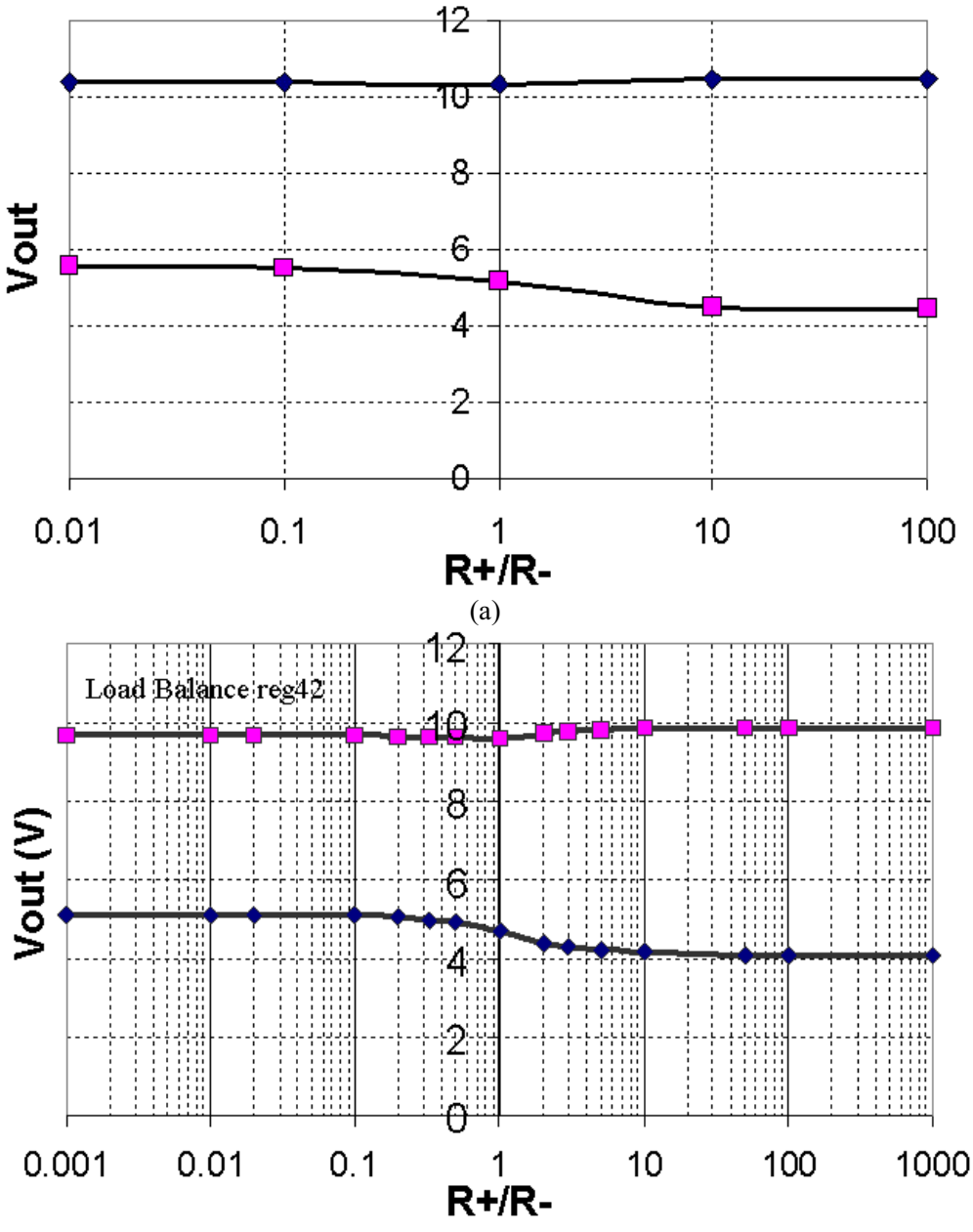


Fig. 19: The unity-gain buffer load balance curve in (a) Zener-referenced open-loop regulator, and (b) V_{be}-referenced closed-loop regulator

The development of a wireless interface for the active stimulating probes is continuing. The high leakage currents sometimes seen from the UM BiCMOS process

has been studied in detail and found to be due to the lack of a buried layer in this process, resulting in a very high parasitic collector resistance in the bipolar devices. Altering the npn transistor geometry and deliberately adding base resistance to the structure have been shown to greatly reduce the problem. Diode-connected MOS transistors can also be used in place of the bipolar devices in the rectifier and can yield very good performance. During the coming term, we will test the complete Interestim-1 and Interestim-2 microsystems. We will also develop a transmitter and PC-based command generator to implement a full wireless stimulation system and test it in-vitro.